Dual 4x4 Low Resistance Analog Switch Array Chip CH449

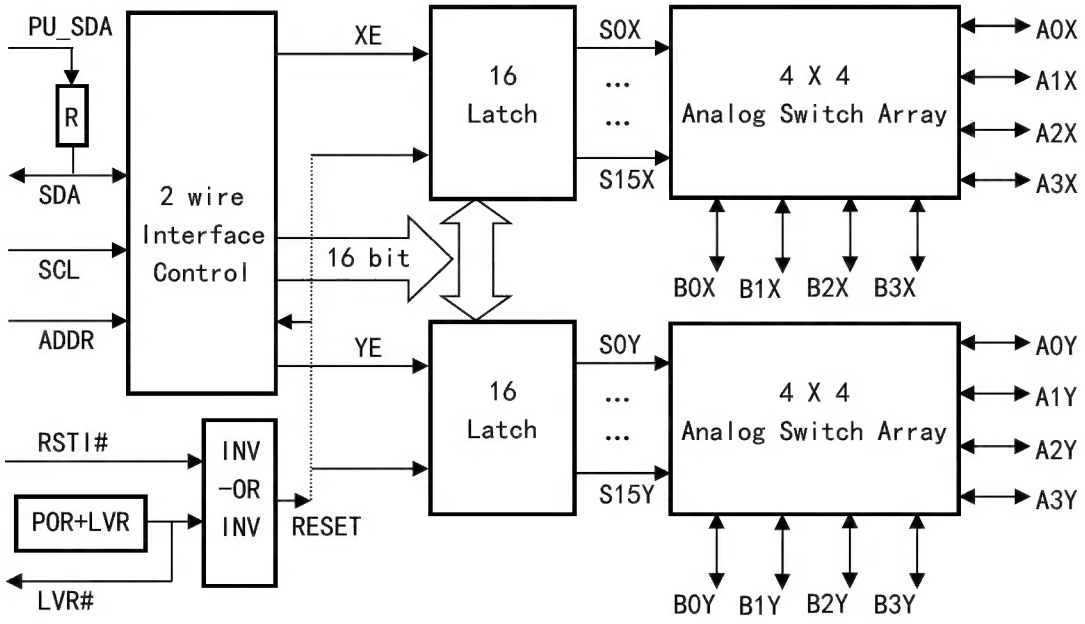
Datasheet
Version: 1A
http://wch.cn

1. Overview

CH449 is a 4x4 matrix differential signal analog switch chip. CH449 contains 32 analog switches, which are divided into two groups and distributed at each cross-point of dual 4x4 signal channel matrices. Each analog switch can be turned on/off independently, so as to implement any dynamic connection of 4x4 differential signal channels.

CH449 supports 5V rated supply voltage, with high bandwidth and low ON resistance, and supports 3.3V or lower supply voltage, can be used for dynamic switch and combination switch between four inputs and four outputs of video or USB2.0 differential signals. For USB3.0, DP1.4 and 5Gbps differential signal matrix analog switch, please refer to CH9444/CH9445 datasheet.

The CH449 series includes CH449F and CH449X. CH449F uses NMOS and PMOS to implement analog switch, and supports the rail-to-rail full-amplitude analog signal. CH449X uses NMOS to implement analog switch, with higher bandwidth, and only supports analog signals with voltage lower than VDD-1.4V. When CH449X is used for signal switch, it can prevent the current from flowing back to VDD by external electrical signals after power down.



2. Features

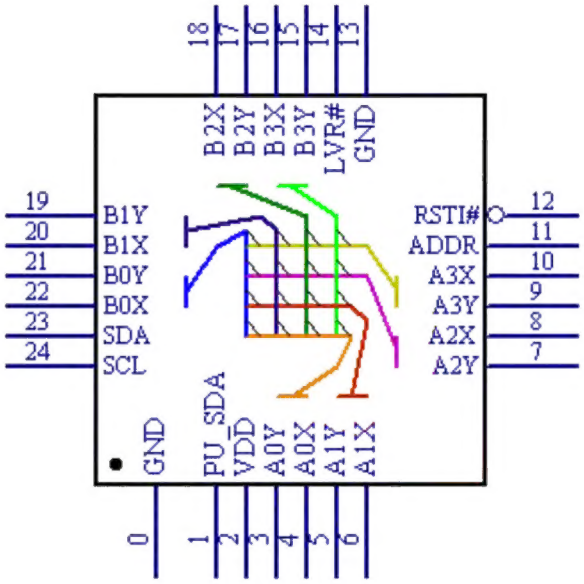
- A dual 4x4 cross-point matrix analog switch, supports four-in four-out differential signal switch.
- Supports switch of two groups of independent four-in four-out single-ended signals.
- Low ON resistance, Ron typical value of about 5 Ω.
- High bandwidth. Supports video signal, low-speed, full-speed and high-speed USB signals.
- 2KV HBM ESD.
- Compatible with IIC two-wire serial control interface. 2 sets of device addresses for selection.
- Built-in power on reset and low voltage reset. Supports external input reset.

- The voltage of all control signals is independent of the supply voltage. Supports 5V, 3.3V, 2.5V and 1.8V control signals.
- Wide supply voltage range. Low static power dissipation. Supports 5V rated supply voltage, power supply can be down to 2.5V.
- Package: QFN24, compatible with RoHS.

3. Package

Package	Body size		Lead pitch		Description	Part No.
QFN24	4*4mm		0.50mm	19.7mil	Quad no-lead 24-pin	CH449F
QFN24	4*4mm		0.50mm	19.7mil	Quad no-lead 24-pin	CH449X

Note: For QFN package, the EPAD is marked as 0# pin, which is unnecessary but recommended to connect.



4. Pin definitions

Pin No.	Pin Name	Pin Type	Description
2	VDD	Power	Positive power
13, 0	GND	Power	Ground, digital signal reference ground
24	SCL	Input	Clock input of 2-wire serial interface
23	SDA	Input and open-drain output	Data input and response output of 2-wire serial interface Built-in controllable pull-up resistor
1	PU_SDA	Input	2-wire serial interface SDA pull-up resistor enable: Low level - built-in resistor disabled; High level - built-in resistor enabled.
11	ADDR	Input	Device address selection input of 2-wire serial interface
12	RSTI#	Input	External reset input, active low
14	LVR#	Open-drain output	Internal low voltage reset output, active low, used for low voltage monitor
4, 3	A0X, A0Y	Analog signal	Terminal 0# of analog switch array port A

6, 5	A1X, A1Y	Analog signal	Terminal 1# of analog switch array port A
8, 7	A2X, A2Y	Analog signal	Terminal 2# of analog switch array port A
10, 9	A3X, A3Y	Analog signal	Terminal 3# of analog switch array port A
22, 21	B0X, B0Y	Analog signal	Terminal 0# of analog switch array port B
20, 19	B1X, B1Y	Analog signal	Terminal 1# of analog switch array port B
18, 17	B2X, B2Y	Analog signal	Terminal 2# of analog switch array port B
16, 15	B3X, B3Y	Analog signal	Terminal 3# of analog switch array port B

5. Functional specification

5.1. Analog switch array

The 4x4 differential matrix switch of CH449 includes two completely independent analog switch arrays X and Y. Each switch array has four ports A and four ports B. Each cross-point of 4*4 matrix has an analog switch. The S0X-S15X codes are used for the channel X, and the S0Y-S15Y codes are used for the channel Y. These analog switches are OFF by default after reset, and combinations can be set to ON/OFF by the external MCU through a 2-wire control interface.

Analog switch codes for the channel X:

X matrix	B0X pin	B1X pin	B2X pin	B3X pin
A0X pin	S0X	S1X	S2X	S3X
A1X pin	S4X	S5X	S6X	S7X
A2X pin	S8X	S9X	S10X	S11X
A3X pin	S12X	S13X	S14X	S15X

Analog switch codes for the channel Y:

Y matrix	B0Y pin	B1Y pin	B2Y pin	B3Y pin
A0Y pin	S0Y	S1Y	S2Y	S3Y
A1Y pin	S4Y	S5Y	S6Y	S7Y
A2Y pin	S8Y	S9Y	S10Y	S11Y
A3Y pin	S12Y	S13Y	S14Y	S15Y

5.2. Two-wire serial control interface

The two-wire serial interface implements transfer through SCL and SDA signal lines. SCL is a clock line, and SDA is a serial data line. Always MSB-first for serial data shift. A complete control command consists of a command and 16-bit data (including start bit, device address and command byte, response 1, high 8-bit switch data, response 2, low 8-bit switch data, response 3 and stop bit).

The lowest bit of device address and command byte is the command bit. CH449 only supports the operation with command bit of 0. The high 7 bits are the 7-bit device address selected by ADDR pin, which cannot be suspended.

When ADDR pin is at low level, the address ranges from 0x19 to 0x1B, the device address and command byte are 0x3X. When ADDR pin is at high level, the address ranges from 0x29 to 0x2B, and the device address and command byte are 0x5X.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
Format	0	ADDR	!ADDR	1	0	YE	XE	0	! ADDR refers to the inverse of the ADDR state
Example 1	0	ADDR	!ADDR	1	0	0	1	0	Set S15X ~ S0X of channel X

Example 2	0	ADDR	!ADDR	1	0	1	0	0	Set S15Y ~ S0Y of channel Y
Example 3	0	ADDR	!ADDR	1	0	1	1	0	Simultaneously set S15 ~ S0 of channels X and Y

The high 8-bit switch data and the low 8-bit switch data constitute the 16-bit switch data. CH449 confirms to save the 16-bit data and apply it to the channel X+Y or X or Y according to the device address and XE/YE in the command byte. When the data bit is 1, the corresponding analog switch is on. When the data bit is 0, the corresponding analog switch is off. The switches can be combined in any way, but need to avoid short circuits between several signal sources. For example, A0 and A2 are on when S0, S3 and S11 are 1, A0 and B0 are on, A0 and B3 are on, A2 and B3 are on.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
High 8-bit data	S15	S14	S13	S12	S11	S10	S9	S8	Each bit corresponds to a switch of the matrix cross-point , and can be combined in any way
Low 8-bit data	S7	S6	S5	S4	S3	S2	S1	S0	

In the differential signal switch matrix application, the channels X and Y should be set uniformly, and the differential signals X and Y can be set to +/- (p/n) or the inverse according to PCB design optimization requirements.

The PU_SDA pin is used to enable the built-in SDA pull-up resistor of CH449. In the application of MCU with built-in pull-up resistor or external pull-up resistor, PU_SDA should be shorted to GND, to disable the built-in pull-up resistor. The PU_SDA pin cannot be suspended.

5.3. Power and reset

CH449 digital pins include SCL, SDA, ADDR, PU_SDA, RSTI#, and LVR#. These pins support 5V-tolerant, and the input voltage can be independent of CH449 supply voltage (VDD).

ADDR is usually connected to GND or VDD as required, and PU_SDA is usually connected to GND or VDD as required.

SCL and SDA are usually driven by the I/O of the external MCU, and CH449 allows the MCU to use a supply voltage which is different from the supply voltage of CH449.

Combinations of CH449 supply voltage and digital pin control voltage		CH449 supply voltage (VDD), maximum voltage of analog signal		
		5V	3.3V	2.5V
I/O voltage of MCU (Voltage on CH449 digital input pins)	5V	√	√	√
	3.3V	Function support	√	√
	2.5V	Function support	Function support	√
	1.8V	×	Function support	Function support

Note: “Function support” in the table above means that the function can be implemented completely, but CH449 may have a static power dissipation of not more than 400uA.

The RSTI# pin is used to input the external reset signal, active low. All analog switches will be turned off after reset. It can be connected to VDD when the external reset input is not required. The RSTI# pin cannot be suspended.

During I/O switch in a dual power system, RSTI# can be connected to power supply of the other party, to automatically reset CH449 when its own power is on but the other party is powered off, so as to turn off all analog switches and all I/Os. If CH449X is used, it can prevent the current from back flowing to VDD through PMOS analog switch when its own power is off but the other party is powered on.

In the application of MCU I/O with only 3.3V supply voltage but 5V external signal voltage, CH449X can also be connected to I/O link in series after supplied by 5V power, so that it has the voltage withstand capacity to the external 5V signal. The voltage of 5V signal is decreased to below 3.6V by CH449X with 5V power supply, and the voltage of 3.3V signal is decreased to below 2.2V by CH449X with 3.3V power supply.

The LVR# pin is the internal low voltage reset output, active low. LVR# outputs low level when VDD supply voltage is lower than VR. It can also be shorted to VCC, to discharge VDD when VDD power is off or when at low voltage.

6. Parameters

6.1. Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃
VDD	Supply voltage (VDD connects to power, GND connects to ground)	-0.5	6.5	V
VANA	Voltage on analog input/output pins of CH449F	-0.5	VDD+0.4	V
VANAN	Voltage on analog input/output pins of CH449X (not related to VDD)	-0.5	6.5	V
VIOD	Voltage on digital input/output pins (not related to VDD)	-0.5	6.5	V
Isw	Continuous through current of analog switch	0	30	mA
Iall	Total continuous through current of all analog switches	0	120	mA

6.2. Electrical characteristics at 5V

Test conditions: TA=25℃, VDD=5V

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VDD	Supply voltage	4.0	5.0	5.5	V
ICC	Static supply current, with all digital pins connected to VDD or GND		2	10	uA
ICCX	Static supply current, with all digital pins at 1.8V		0.5	2	mA
VIL	Low level input voltage of digital pins	0		1.1	V
VIH	High level input voltage of digital pins	2.2		5.5	V
ILEAK	Input leakage current of digital pins		0.1	10	uA
IUSDA	Pull-up current of SDA pin with internal resistor enabled	250	500	700	uA
ILSDA	Low level absorption current of SDA pin @SDA=0.5V	4	5.5		mA

VR	Default power on reset threshold	1.8	2	2.2	V
ILVR	Absorption current of LVR# pin during reset (shorted to VDD)	0	21	55	mA
IOFF	Leakage current of analog switch in off state		±0.05	±1	uA
VANA	Recommended voltage range of analog signal	0		2.8	V
VANAX	Allowed voltage range of analog signal of CH449F	-0.3		VDD+0.3	V
VANAN	Allowed voltage range of analog signal of CH449X	-0.3	<VDD-1.8	VDD-1.4	V
RON1	Analog switch ON resistance, with analog signal voltage of 0V		4	7	Ω
RON2	Analog switch ON resistance, with analog signal voltage of 2V		6	10	Ω
RON3	CH449F switch ON resistance, with signal voltage of 3.4V		10	15	Ω
RON4	CH449F switch ON resistance, with signal voltage of 5V		6	10	Ω
RON5	CH449X switch ON resistance, with signal voltage of 3.2V		80	120	Ω
RON6	CH449X switch ON resistance, with signal voltage of 3.5V		5K		Ω

6.3. Electrical characteristics at 3.3V

Test conditions: TA=25°C, VDD=3.3V

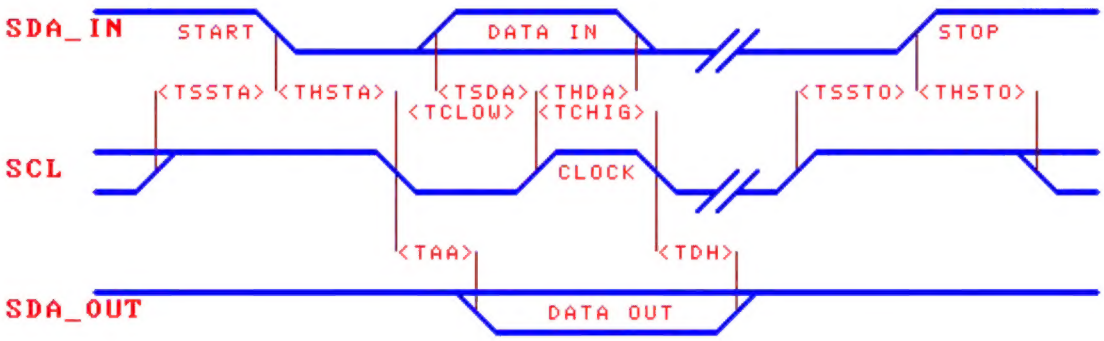
Symbol	Parameter description	Min.	Typ.	Max.	Unit
VDD3	Supply voltage	2.1	3.3	3.9	V
ICC3	Static supply current, with all digital pins connected to VDD or GND		1	5	uA
ICCX3	Static supply current, with all digital pins at 1.3V		0.2	1	mA
VIL3	Low level input voltage of digital pins	0		0.7	V
VIH3	High level input voltage of digital pins	1.8		5.5	V
ILEAK3	Input leakage current of digital pins		0.1	5	uA
IUSDA3	Pull-up current of SDA pin with internal resistor enabled	100	210	300	uA
ILSDA3	Low level absorption current of SDA pin @SDA=0.5V	2.5	3.8		mA
VR	Default power on reset threshold	1.8	2	2.2	V
ILVR3	Absorption current of LVR# pin during reset (shorted to VDD)	0	21	40	mA
IOFF3	Leakage current of analog switch in off state		±0.02	±0.5	uA
VANA3	Recommended voltage range of analog signal	0		1.5	V
VANAX3	Allowed voltage range of analog signal of CH449F	-0.3		VDD3+0.3	V
VANAN3	Allowed voltage range of analog signal of CH449X	-0.3	<VDD3-1.5	VDD3-1.1	V

RON1	Analog switch ON resistance, with analog signal voltage of 0V		5	9	Ω
RON2	Analog switch ON resistance, with analog signal voltage of 1.2V		10	14	Ω
RON3	CH449F switch ON resistance, with signal voltage of 2.0V		20	28	Ω
RON4	CH449F switch ON resistance, with signal voltage of 3.3V		8	12	Ω
RON5	CH449X switch ON resistance, with signal voltage of 1.8V		45	70	Ω
RON6	CH449X switch ON resistance, with signal voltage of 2.1V		4K		Ω

6.4. Interface timing parameters

Test conditions: TA=25℃, VDD=5V or VDD=3.3V, Refer to the attached figure

Symbol	Parameter description	Min.	Typ.	Max.	Unit
TSSTA	Setup time of SDA falling edge start signal	100			nS
THSTA	Hold time of SDA falling edge start signal	100			nS
TSSTO	Setup time of SDA rising edge stop signal	100			nS
THSTO	Hold time of SDA rising edge stop signal	100			nS
TCLOW	Low level width of SCL clock signal	100			nS
TCHIG	High level width of SCL clock signal	100			nS
TSDA	Setup time of SDA input data to SCL rising edge	30			nS
THDA	Hold time of SDA input data to SCL rising edge	20			nS
TAA	Delay of SDA output data valid to SCL falling edge	5		40	nS
TDH	Delay of SDA output data invalid to SCL falling edge	5		60	nS
Rate	Average data transfer rate	0		2M	bps



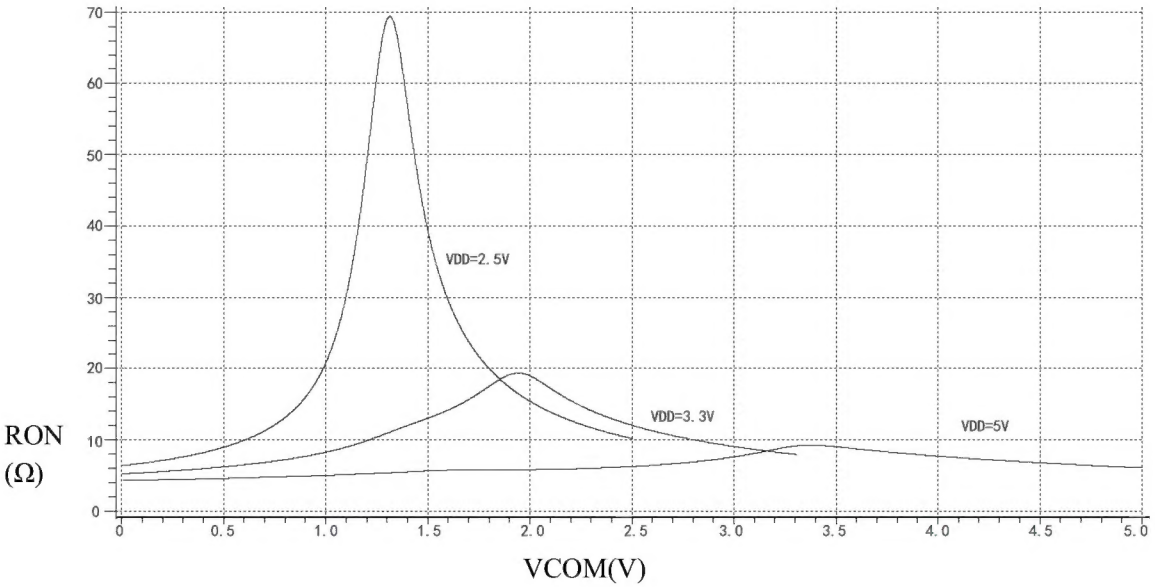
6.5. Other timing parameters

Test conditions: TA=25℃, VDD=5V, VANA=0V, F=1MHz)

Symbol	Parameter description	Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitance		3	8	pF
COFF	Analog signal pin capacitance when CH449F switch is off		7	10	pF
CON	Analog signal pin capacitance when CH449F switch is on		10	15	pF
BW	CH449F analog switch -3dB bandwidth	350	500		MHz
COFFN	Analog signal pin capacitance when CH449X switch is off		4	7	pF
CONN	Analog signal pin capacitance when CH449X switch is on		6	11	pF
BWN	CH449X analog switch -3dB bandwidth	500	800		MHz

6.6. Characteristic diagram

6.6.1 Correlation between CH449F analog switch ON resistance RON and analog signal voltage VCOM (TA=25°C)



7. Applications

7.1. Switch of several video signals

The CH449 features high bandwidth and low resistance, more suitable for video signal switch, such as selection from several video sources.

As the analog circuit and the digital circuit share VDD and GND, the GND pin must be in good connection, to reduce interference. The VDD pin must connected to an external decoupling capacitor. It is recommended to appropriately reduce the edge angle of the digital input signal, to reduce transfer frequency.

7.2. Switch of several USB signals

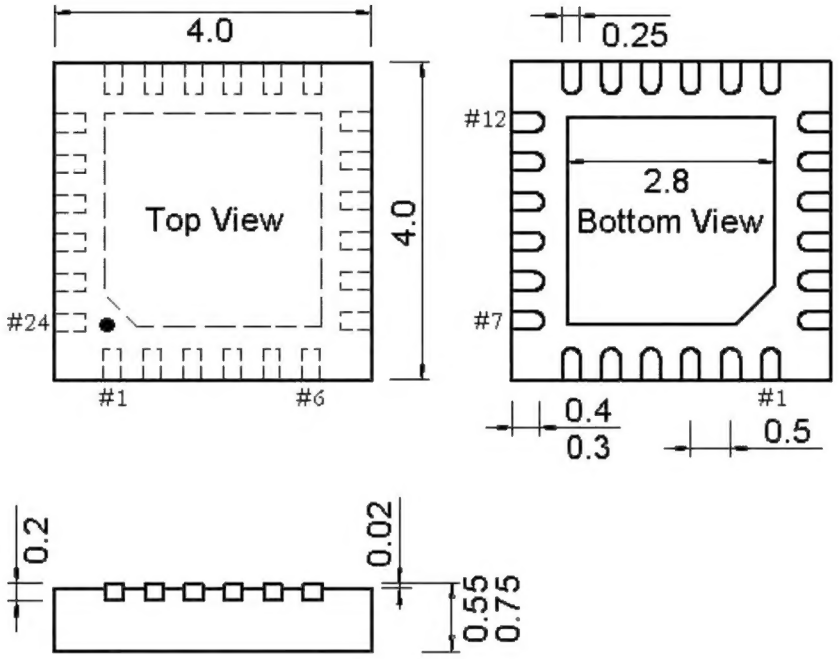
The CH449 supports dynamic reconstruction of 4-channel low-speed, full-speed and high-speed USB signal connections, to implement physical layer routing. If CH449X is selected, VDD should be 5V. For matrix switch of SuperSpeed USB3.1 and DP1.4 signals, please refer to CH9444/CH9445 datasheet.

7.3. Digital I/O physical layer routing and I/O expansion

The CH449 can be used for digital signal routing between MCU and external I/O devices, and I/O connection can be dynamically reconstructed to implement function switch.

When MCU I/O is not enough, CH449 can be used to expand the low-speed output port (connected to external GND or VDD).

8. Package information

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, and the error of other dimensions is not more than ±0.2mm.

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